

Utilization of COTS Electronics in Space Application, Reliability Challenges and Reality

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Abstract - The utilization and application of commercially available semiconductor devices in high reliability space systems requires a thorough understanding of not only the reliability and failure mechanisms associated with the selected devices, but also of qualification and characterization methods to determine the suitability of these devices to the intended application. This paper provides a description of common reliability and qualification practices and methods related to the utilization of Commercial-Off-The-Shelf (COTS) microelectronics in critical space applications.

I. INTRODUCTION

The semiconductor industry has experienced drastic changes in the last ten years with tremendous growth in market competition resulting in substantial improvements in processing methods, design capability, performance improvements, fabrication yield, and overall quality of commercially viable devices. This coupled with large volume production and the utilization of statistical process control has greatly reduced the variability of a process and positively impacted the infant mortality population. However, reproducibility of a product does not guarantee reliability in the intended application. For critical space applications where the success or failure of a mission hinges on the lifetime and performance of a single device; it is critical that all aspects of the reliability and the various known failure modes and mechanisms be addressed prior to the insertion of the component in the application [1].

The selection and application of microelectronic components in high reliability space systems requires knowledge of the component design, fabrication process, and applicable tests. In addition, reliability analysis and detailed knowledge of the application environment is necessary in order to determine the suitability of the selected component for the application. These issues are of particular importance for the application of commercially available microelectronic devices in high reliability systems due to the need for the utilization of these devices at the upper limit of their performance and environmental tolerance capabilities.

The high reliability user of microelectronic devices developed for the commercial sector must gain an

understanding of not only the technology performance capabilities but also of the limitations of the technology and must employ methods to utilize it in a reliable fashion. The user must also understand that new failure mechanisms, not previously encountered, could impact the reliability of new designs and materials. In addition, many of the traditional assumptions for mean-time failure rate predictions do not hold for those new devices. Thus, today's high reliability user must be more aware of qualification and characterization methods of commercial products in order to determine suitability for the intended application.

II. RELIABILITY PREDICTION

The quantitative determination of device reliability involves probability statistics, time, and a definition of failure. Given a failure criterion, the most direct way to determine reliability is to submit a large number of samples to actual use conditions and monitor their performance against the failure criteria over time. Since most applications require device lifetimes of many years, this approach is not practical. To acquire device reliability data in a reasonable amount of time, an accelerated life test at either high temperature or other acceleration factor is used. In general, the high temperature condition is used based on the observation that most failure mechanisms are thermally activated. By exposing the devices to elevated temperatures, it is possible to reduce the time to failure of a component, thereby enabling data to be obtained in a shorter time than would otherwise be required. Such a technique is known as "accelerated testing" and is widely used throughout the semiconductor industry. The rate at which many chemical processes take place is governed by the Arrhenius equation:

$$R = A \exp(-E_a/kT)$$

where

R = rate of the process

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E_a = activation energy, a constant

k = Boltzmann's constant, 8.6×10^{-5} (eV/K)

T = Absolute temperature in Kelvin

This equation has been adopted by the semiconductor industry as a guideline by which the operation of devices under varying temperature conditions can be monitored. Experimental data obtained from life tests at elevated temperatures are processed via the Arrhenius equation to obtain a model of device behavior at normal operating temperatures. Rearranging the Arrhenius equation allows the temperature dependence of component failure to be modeled as follows:

$$\ln t_2/t_1 = E_a/k (1/T_2 - 1/T_1)$$

where

$t_{1,2}$ = time to failure

E_a = activation energy in electron volts

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III. COTS QUALIFICATION

Qualification can be defined as the verification that a particular component's design, fabrication, workmanship, and application are suitable and adequate to assure the operation and survivability under the required environmental and performance conditions.

Traditional qualification methods require extensive test and characterization of the specific component using a predetermined set of tests and characterization conditions. This approach can be very costly in schedule and expense but can result in meaningful qualification and reliability data for the specific application.

A methodology for qualification based on continual interaction between the device manufacturer and the user is the desired state. However, for most high reliability applications, the quantity of the required devices is very limited, forcing the user to procure the required devices indirectly through a distributor which eliminates the desired interaction. For large volume users, this interaction results in a detailed understanding of the device design, fabrication, and limitations along with the specific application conditions and expected operating environment. In general, the methodology is divided into three main categories; Process Qualification, Product Qualification, and Product Acceptance. The first two categories are very helpful, but are only practical for large volume users. The last category is the only viable option for most high reliability, low volume users.

Process Qualification: Is a set of procedures the manufacturer follows to demonstrate the control of the entire process of design and fabrication using a specific technology. It addresses all aspects of the process including the acceptance of starting materials, documentation of

procedures, implementation of handling procedures and the establishment of lifetime and failure data for devices fabricated using the process. Since the goal of process qualification is to provide assurance that a particular process is under control and known to produce reliable parts, it is typically performed only once, although routine monitoring of the production line is standard. In addition, any significant changes in the process may require re-qualification of the process. It is critical to remember that only the process and basic circuit components are being qualified. No reliability information is obtained for particular component designs.

Although process qualification is intended to qualify a defined fabrication procedure and device family, it must be understood that the technology is constantly evolving, and this technology evolution requires the continual change of fabrication procedures. Thus, strict application of the commonly used phrase, "freezing the production process," does not apply.

The qualification process also involves a series of tests designed to characterize the technology being qualified. This includes the electrical as well as the reliability characteristics of components fabricated on the line. Some of these tests are performed at wafer level and include the characterization of Process Monitors (PM), and Technology Characterization Vehicles (TCV).

In reality, the manufacturer will already have an existing and defined process with established reliability and qualification procedures and practices. Therefore, it is the user's responsibility to become knowledgeable of these practices and to become aware of the necessary qualification steps. All of these tests and the applicable procedures are an integral part of the qualification program and provide valuable reliability and performance data at various stages in the manufacturing process.

The only practical option for the low volume high reliability user is to review available process qualification data from the manufacturer to determine suitability and applicability to the specific component in question.

Product Qualification: is the verification that a component will satisfy the design and application requirements under the specified conditions. The information sought-after in this approach is design specific and applies to devices fabricated on qualified process lines. This qualification step is composed of Design Verification and Product Characterization.

Verification of custom designs is one of the best ways of reducing engineering costs and improving reliability. Design reviews with the participation of the device manufacturer and the device user are a means of accomplishing this verification of model or simulation and layout of the design prior to fabrication. Verification of circuit design is only

applicable to custom designs and requires detailed knowledge of the design tools, device physics, layout tools, fabrication and test which requires the participation of personnel from the various disciplines.

Most manufacturers of COTS devices typically verify the design prior to fabrication and utilize their standard design and fabrication rules with specific performance conditions desired for the product. Some or all of this information may be available to high volume users, but is seldom available to low volume users such as the high reliability user.

Product characterization is another important aspect of product qualification. Thermal analysis and tests to determine the thermal characteristics of the design, along with ESD sensitivity tests, voltage ramp tests, and temperature ramp tests are all essential in obtaining an understanding of the limitations and characteristics of the design. These characterizations are applicable to both custom and standard designs and are an accepted practice for establishing product qualification. However, each manufacturer will utilize their standard set of characterization conditions to satisfy the intended commercial application and performance window.

The difference in the characterization criteria and conditions is an area having a direct impact to the user of COTS devices in high reliability applications.

Product Acceptance: Although devices may be designed by highly qualified personnel, fabricated on a process qualified production line, and verified through measurements to meet the design goals; parts with poor reliability characteristics still may exist. This may be due to variations in the fabrication process, or material flaws that were undetected, or, as is more often the case, to the device package and stress imposed on the device during packaging. Regardless of the cause, these weak devices must be found and removed before they are integrated into the system. Therefore, manufacturers of high reliability systems require the devices to pass a series of product acceptance screens, whose sole purpose is to increase the confidence in the reliability of the devices. This step in the qualification methodology is the major difference between space-qualified devices and commercial grade devices.

The level of testing performed under product acceptance is a function of the form of the deliverable. For example, the first level of acceptance testing, called "wafer acceptance test" is performed at the wafer level to assure the uniformity and reliability of the fabrication process through a wafer-to-wafer comparison. "Lot acceptance test for die" is a second level of testing that provides further reliability information, but only on a sample of the devices because of the difficulty in performing full characterization on non-packaged devices. "Packaged device screen" is performed on 100% of the devices if the deliverable is a packaged product. This level

of testing should reflect the intended application conditions and also take into account the information gained in the product characterization step.

For most low volume users of COTS devices, test and characterization of devices in their final packaged form is the only available option to empirically assess the suitability of the product to the intended application. The challenge resides in the applied test conditions and interpretation of the resultant data. Here, knowledge of the device design, construction and fabrication process becomes critical to the actual conditions utilized during test. For screening tests, one must design the tests with the objective of detecting failure mechanisms affecting infant mortality under normal operating conditions. Consideration must be given to the bias conditions during test vs. those during operation. In addition, thermal and mechanical test conditions must also be considered to reflect those used during normal operation. A pre-defined failure criteria and test parameters are a must prior to initiation of the screens.

Standard practices at JPL require COTS devices to successfully satisfy a screening test and a detailed regiment of characterization tests prior to utilization in the final design [2]. This approach is designed with consideration for the component's design limits and the actual application conditions and environment. For plastic encapsulated microcircuits, special consideration is given to thermal limits and burn-in conditions in order to maintain the integrity of the components in question [3].

Construction analysis and destructive physical analysis are typically utilized to help the user in understanding the construction and workmanship of the components in question. A number of user organizations tend to utilize this step very early in the selection cycle in order to provide insight into the suitability of the component for the application prior to initiation of any tests.

Special Environments: For most space applications, the user must consider how the selected component will operate under the expected environment. Since COTS components are designed for an earth-like environment, special consideration and characterization may be necessary to determine the suitability of the selected COTS component for the intended space application. Three main environmental conditions must be considered; the radiation environment, the thermal environment, and the mechanical shock environment.

The mechanical shock environment relates primarily to the shock experienced during launch. Both analytical and experimental techniques can be utilized to determine suitability of the component to the expected launch environment. Other shock environments could relate to missile applications and the same techniques can be utilized.

For some space applications, it may be necessary to operate devices at thermal conditions beyond those experienced in normal operation on earth. For example; operation conditions on the surface of Mars may require the devices to operate in a cyclical mode at temperatures as low as -140°C and as high as $+40^{\circ}\text{C}$. This environment may present a very difficult challenge to most COTS devices not designed to withstand such an environment. Therefore, a characterization test regiment is typically designed to assess the components performance and any failures as a result of operation under those conditions.

Lastly, most COTS devices are designed to operate in a benign earth environment and are not intended to withstand the radiation environments of space. Electrons, protons and ions in space can cause permanent damage in some types of electronic devices that can lead to operational failure. Utilization of COTS devices in space applications necessitates test and characterization of devices to determine their performance under a specific radiation environment and test conditions.

Figure 1 illustrates the how the current transfer ratio – the critical parameter for optocouplers – varies among various lots of 4N49-type optocouplers. The key point is that there are large lot-to-lot variations. The two date codes produced in 2001 are considerably different, and are so severely degraded by proton fluence equivalent to about 2 krad (Si) that lot sampling is required in order to use these devices in most space systems.

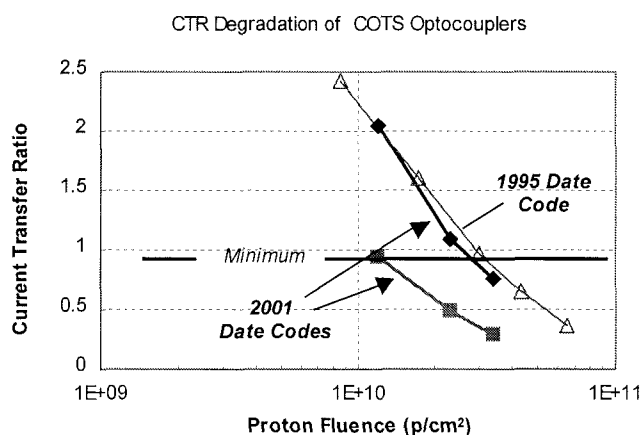


Figure 1. Radiation effect on the current transfer ratio for 4N49-type optocoupler from 2 different date codes [4].

The main difficulty faced by high reliability users is that COTS manufacturers may implement a processing change resulting in a small performance impact in an earth environment, but a serious impact under a space radiation environment. This presents a very serious obstacle to wide utilization of COTS devices in space systems.

Figure 2 illustrates the gain degradation of several lots of JANTX2222A transistors, which are frequently used in space systems. The earlier lot of devices was procured in 1993 while the other two lots procured at a later date are far more degraded, particularly at higher total dose levels. This illustrates the importance of lot-sample testing. Note that these transistors are not specifically controlled or hardened for radiation environments, even though they are qualified to “JANTX” specifications. Thus, even though they are not strictly “COTS” devices their radiation behavior is no different from other commercial components.

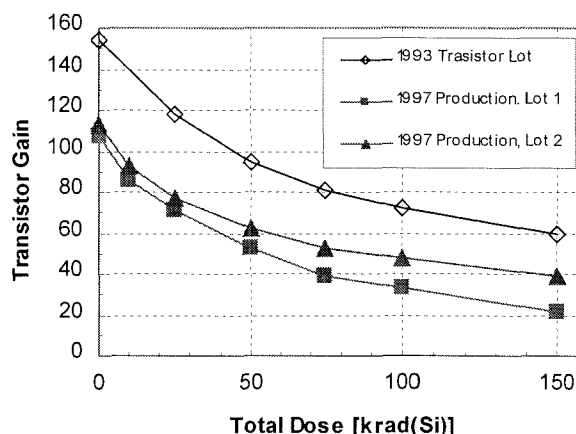


Figure 2. Lot variations as evident in degradation of the transistor gain for JANTX2222A from 3 different lots [5].

Standard practices at JPL require all parts to be evaluated for radiation Total Ionizing Dose (TID), Displacement Damage (DD) and Single Event Effect (SEE) sensitivity, relative to the radiation requirements of the specific application. Where no radiation data are available, all candidate radiation-sensitive parts are required to undergo characterization testing and/or lot acceptance testing or be shown by analysis based on test data to be compatible with the application radiation levels. Radiation data should show 90% confidence that the population probability of survivability is at least 99%. This is a very time consuming and costly option, but given the wide variability in the radiation tolerance of microelectronic devices designed for the commercial sector, it is the only viable option.

IV. SUMMARY

In order to achieve the high performance needs of space systems, the utilization of COTS components for space applications has become a must. However, not all COTS may be suitable for utilization in space applications with the burden of proof being on the user and not the manufacturer.

Techniques and methods for test and characterization of COTS devices to determine suitability to space application have been developed by a number of users with the emphasis on the intended application and environment. However, the main difficulty remains in analysis of test results to determine long-term reliability.

One of the most difficult obstacles for wider utilization of COTS components in space systems is the large variability in response to the effects of radiation.

V. ACKNOWLEDGMENT

The work described in the paper was conducted at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration.

VI. REFERENCES

- [1] S. Kayali, Reliability of Compound Semiconductor Devices for Space Applications, Microelectronics Reliability Vol. 39, (1999).
- [2] Institutional Parts Program Requirements, JPL publication D-20384.
- [3] Plastic Encapsulated Microcircuits (PEMS) Reliability/Usage Guidelines for Space Applications, JPL publication D-19426.
- [4] B. Rax, C. Lee, A. Johnston and C. Barnes, "Total Dose and Proton Damage in Optocouplers," IEEE Trans. Nucl. Sci., vol. 43, pp 3167 (1996).
- [5] A. Johnston, G. Swift, and B. Rax, "Total Dose Effects in Conventional Bipolar Transistors and Integrated Circuits," IEEE Trans. Nucl. Sci., vol. 41, pp 2427, (1994).

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I. INTRODUCTION

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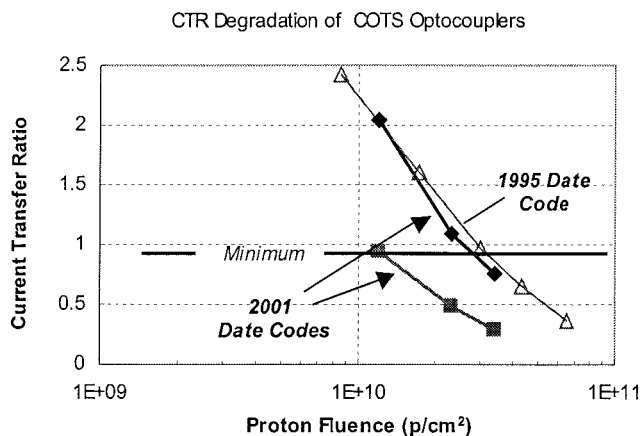


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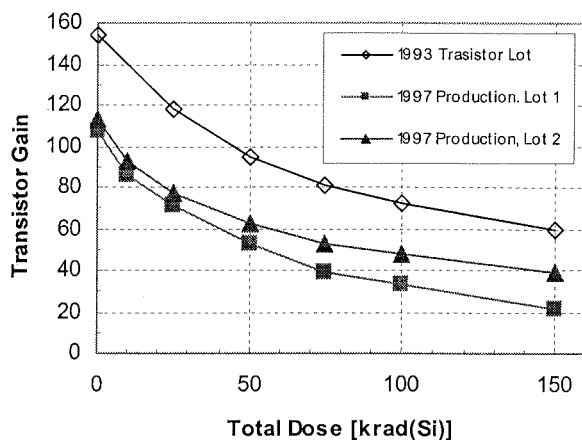


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IV. SUMMARY

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V. ACKNOWLEDGMENT

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- [2] JPL Internal Document D-20384.
- [3] JPL Internal Document D-19426.
- [4] B. Rax, C. Lee, A. Johnston and C. Barnes, "Total Dose and Proton Damage in Optocouplers," IEEE Trans. Nucl. Sci., vol. 43, pp 3167 (1996).
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